

 <div data-bbox="491 98 536 264" style="display: inline-block; vertical-align: middle;"> <b>I Q R</b> </div>	IBIS QUALITY REPORT	date	1 (8)
		30-Apr-15	

## IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	m24c32_g6_mlp2x3.ibs
IBIS Version:	4.0

	<b>IBIS QUALITY REPORT</b>	date	2 (8)
		30-Apr-15	

**Contents**

1. MODELING..... 3

1.1 Component description..... 3

1.2 Modeling conditions ..... 3

1.3 Circuit for data extraction ..... 5

2. IBISCHK6 CHECK ..... 6

2.1 Result Check by IBISCHK6 ..... 6

3. FUNCTIONAL CHECK..... 7

3.1 Functional verification..... 7

4. EXTRA INFORMATION ..... 8

	<b>IBIS QUALITY REPORT</b>	date	3 (8)
		30-Apr-15	

# 1. MODELING

IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

## 1.1 Component description

Component reference	Technology	Component description
M24C32-DRE M24C64-DRE M24128-DRE M24256-DRE M24512-DRE	CMOS F8H/P2	The M24xxx-DRE is an I <sup>2</sup> C-bus compatible EEPROM (Electrically Erasable PROgrammable Memory) operating with a supply voltage ranging from 1.8V to 5.5V, over the -40°C to 105°C temperature range.

## 1.2 Modeling conditions

Simulator used	AMS 2010.1 (Mentor Graphics)
----------------	------------------------------

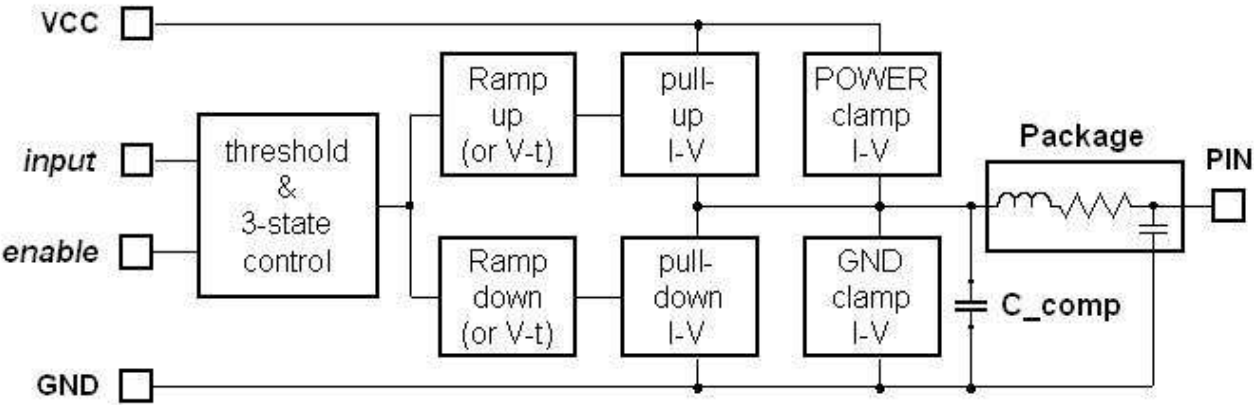


Figure 1: IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	105
Voltage Supply [Volt]	5.0	4.5	5.5
Process setting	nom	weak	strong

	<b>IBIS QUALITY REPORT</b>	date	4 (8)
		30-Apr-15	

<b>Model names</b> (of Component)	<b>Model Type</b>	<b>C_comp (typ, min, max)</b>
mod_sda	I/O_Open_Drain	2.925pF (typ), 2.793pF(min) , 3.207pF (max)
mod_scl	Input	2.193pF (typ), 2.023pF (min) , 2.323pF (max)
mod_en	Input	2.193pF (typ), 2.023pF (min) , 2.323pF (max)
mod_wc	Input	2.193pF (typ), 2.023pF (min) , 2.323pF (max)

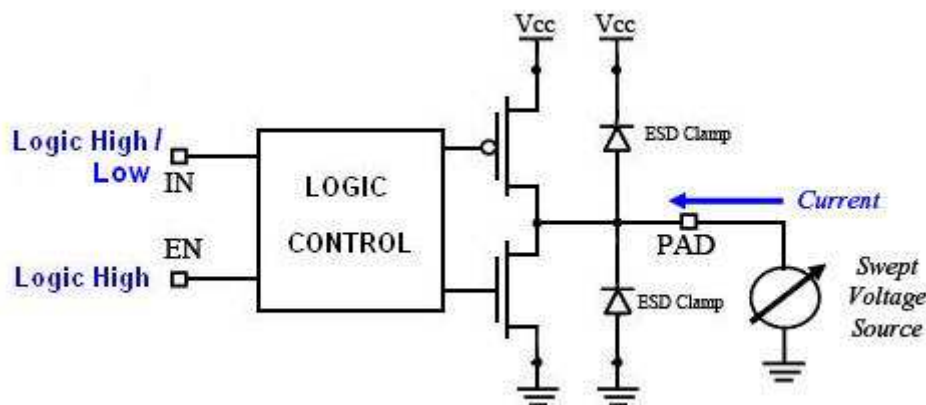
<b>Model names</b> (of Component)	<b>Threshold and Vmeas</b>	<b>Timing parameters (if used)</b>
mod_scl/wc/en	Vil=1.50V , Vih=3.50V	
mod_sda	Vmeas=2.500V	Rref=1kOhm, Cref=10pF, Vref=5.00V

<b>Package</b>	<b>Description</b>
MLP2x3	Micro Leadframe Package 2mm x 3mm (8 leads)

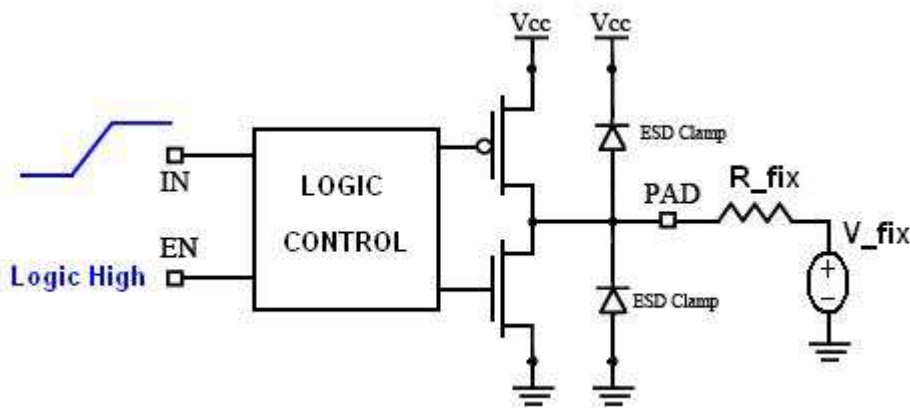
	<b>IBIS QUALITY REPORT</b>	date	5 (8)
		30-Apr-15	

### 1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.



**Figure 2:** Simulation Setup to extract **I/V** data from I/O model type



**Figure 3:** Simulation Setup to extract **V/T** data from I/O model type (see also Table 1)

<b>V/T data condition extractions</b>	<b>Load conditions</b>
Rising waveform	R_fix=50 Ohm, V_fix= 0 V
Rising waveform	R_fix=50 Ohm, V_fix= 5.0 V
Falling waveform	R_fix=50 Ohm, V_fix= 5.0 V
Falling waveform	R_fix=50 Ohm, V_fix= 0 V

**Table 1:** V/T curve extraction load conditions

	<b>IBIS QUALITY REPORT</b>	date	6 (8)
		30-Apr-15	

## 2. IBISCHK6 CHECK

The created IBIS model must be checked using IBISCHK6 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

### 2.1 Result Check by IBISCHK6

*IBISCHK6 V6.0.1*

*Checking m24c32\_g6\_mlp2x3.ibs for IBIS 4.2 Compatibility...*

*NOTE (line 295) - Pulldown Typical data is non-monotonic*

*NOTE (line 296) - Pulldown Minimum data is non-monotonic*

*NOTE (line 296) - Pulldown Maximum data is non-monotonic*

*Errors : 0*

*File Passed*

<b>Adding comments about the Warning or Note:</b>
<p>The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.</p>

	<b>IBIS QUALITY REPORT</b>	date	7 (8)
		30-Apr-15	

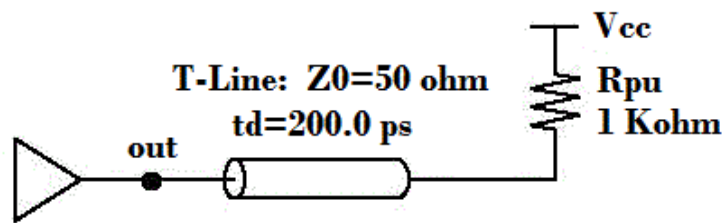
### 3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions ( Figure 4), must match. These output comparisons are presented in TYP, MIN and MAX condition. This section cannot be defined for Input and Terminator model type, because they are input-only model types.

How well results are matched?	Put “X” into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshoot and/or Undershoot regions.	
Curves match well.	X

#### 3.1 Functional verification

Circuit used for output comparison results is illustrated in figure 4.



**Figure 4:** Circuit used for functional check

	IBIS QUALITY REPORT	date	8 (8)
		30-Apr-15	

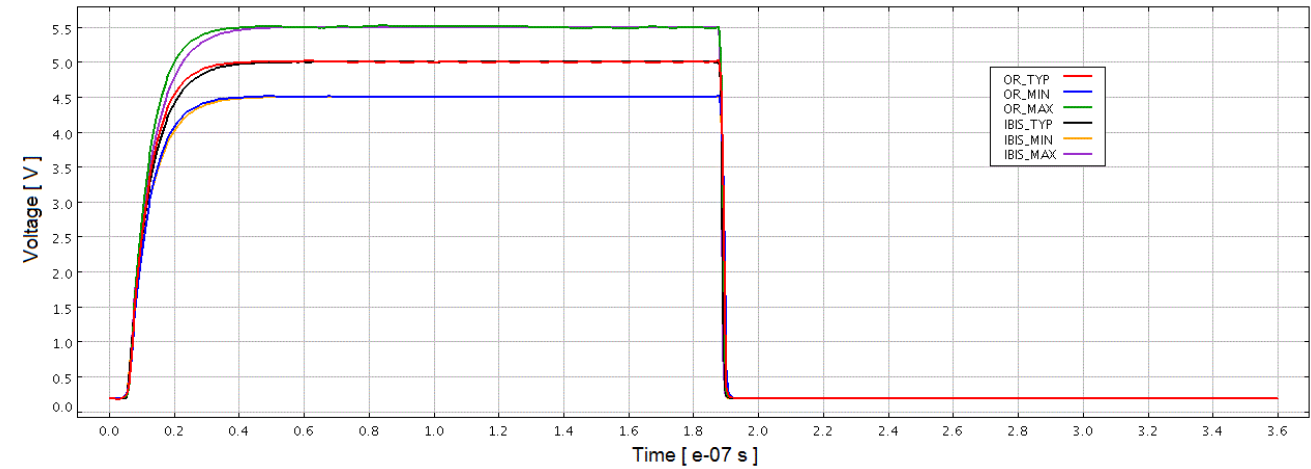


Figure 5: IBIS vs Eldo comparison results of “mod\_sda” Model

Output Comparisons:

Adding comments about the comparison:

#### 4. EXTRA INFORMATION

This section can contains other extra informations, to explain some other features of peculiar IBIS model

Other specifications	description